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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/941,604	08/30/2001	Herlin Chang	CHAN3110/EM/7186	6770

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BACON & THOMAS, PLLC  
625 SLATERS LANE  
FOURTH FLOOR  
ALEXANDRIA, VA 22314

EXAMINER

DEBERADINIS, ROBERT L

ART UNIT PAPER NUMBER

2836

DATE MAILED: 04/22/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/941,604

Applicant(s)

HERLIN CHANG et al.

Examiner

Robert L. DeBeradinis

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on Aug 30, 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-18 is/are pending in the application.
- 4a) Of the above, claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-18 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claims \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on Aug 30, 2001 is/are a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.  
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some\* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
\*See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).  
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). \_\_\_\_\_ 6) ☐ Other:

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## DETAILED ACTION

### *Claim Rejections - 35 USC § 112*

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1, 2, 8-18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 1.

“A first multiple power sources control system ...and main comprises:” it is unclear what main is referring to.

Regarding claim 2.

“...receive two more than two...” it is unclear what is meant, is it two or more than two?

Regarding claim 8.

“...to provide said MOSFET transistor with direction of an electric current;” unclear what is meant.

“... a bridge rectifier, which can ...” can is indefinite.

“...which can provide...” etc.

Regarding claims 6, 8, 9, 10, 12, 14, 15, 16, 18 the applicant uses “can” in the claim language which renders the claims to be indefinite.

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Regarding claims 11, 17.

“...and decide to bias.” unclear what is meant.

***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over THEREZE 5,798,578 in view of KADATSKY 6,381,155.

Regarding claim 1.

THEREZE discloses;

a plurality of power input sides (LM1-LMi) which are used to receive a plurality of external independent power sources (P1-Pi);

a plurality of first voltage and current detecting modules (LM1-LMi) which are used to detect whether said power sources of said power input sides is normal (column 4, lines 53-68);

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a plurality of power output sides (CP1-CPi) which are used to supply a plurality of loads (CH1-CHk) with required power;

a plurality of second voltage and current detecting modules (LC1-LCk), which are used to detect whether power of said power output sides is normal;

a plurality of power source switching modules, which are used to switch a power source supplying said power output sides with power due to a signal of a control module;

said control module (figure 2, U1, U2 etc.) , which control a plurality control switches (Q1, Q2) to be in an ON or OFF state and control said power source switching modules according to a state informed from said first voltage (Vin) and current detecting modules and said second voltage and current detecting module CH1-CHk).

THEREZE does not disclose wherein control module can output a harmonic signal to said input sides.

KADATSKY discloses output ripple factor corresponds to a harmonic when a mismatch of any parameters within any channel occurs.

It would be obvious to one having ordinary skill in the art at the time of this invention to generate a synchronizing signal to reduce the harmonic frequency content generated by ripple in the plurality of power sources to improve ripple filtering (abstract).

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Regarding claim 2.

THEREZE in view of KADATSKY disclose the multiple power sources control system as recited in claim 1, THEREZE discloses wherein there are at least two said power input sides which receive more than two said independent power sources (THEREZE, figure 1, P1, Pi).

Regarding claim 3.

THEREZE in view of KADATSKY disclose the multiple power sources control system as recited in claim 1, THEREZE discloses wherein there is at least one said power output side which can supply one or more than one said loads with power ( THEREZE, column 1, lines 5-24).

Regarding claim 4.

THEREZE in view of KADATSKY disclose the multiple power sources control system as recited in claim 1, THEREZE discloses wherein there is at least one first voltage and current detecting module ( THEREZE, LM MODULES) which detect two or more than two said power inputs sides (FIGURE 2, +Vin, +Vaux).

Regarding claim 5.

THEREZE in view of KADATSKY disclose the multiple power sources control system as recited in claim 1, THEREZE discloses wherein there is at least one second voltage and current system which detect one or more than one said power output sides (column 2, lines 46-68).

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Regarding claim 6.

THEREZE in view of KADATSKY disclose the multiple power sources control system as recited in claim 1, THEREZE discloses wherein said power source switching modules can switch two or more than two said independent power sources ( figure 2, +Vin, +Vaux).

Regarding claim 7.

THEREZE in view of KADATSKY disclose the multiple power sources control system as recited in claim 1, THEREZE discloses wherein there is one or more than one said power source switching modules ( LM1-LMi).

5. Claims 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over THEREZE 5,798,578 in view of JOHNSON 5,185,536 in further view of MATSUMOTO 6,218,810 AND FARRINGTON 6,188,592.

Regarding claim 8.

THEREZE disclose a first power source control module, which comprises:

a MOSFET transistor (Q2) , which controls whether power is transmitted to loads, THEREZE does not disclose a bridge rectifier, a bias circuit or a coupler.

JOHNSON discloses bridge rectifier (42).

MATSUMOTO discloses bias circuit (FIGURE 10) for MOSFET (51).

FARRINGTON discloses coupler (Tsx).

It would have been obvious to one having ordinary skill in the art at the time of this invention to provide a MOSFET transistor, to control whether power is transmitted to a load; a

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bridge rectifier to provide the MOSFET transistor with a DC electric current; a bias circuit to provide a fixed bias for the MOSFET transistor; and a coupler to isolate a control signal from the MOSFET switch to provide power to a load.

Regarding claims 9, 10.

The Examiner takes official notice:

MOSFET transistors and a bi-polar transistors are well know solid state switching devices.

Coupling devices are well known in the art.

It would have been obvious to one having ordinary skill in the art at the time of this invention to select either a MOSFET switching device or a Bi-polar transistor switching deice and to couple the control signal through a coupling device such as a transformer or an optical coupling device to isolate the switching control signal from other parts of the circuit.

6. Claims 13-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over THEREZE 5,798,578 in view of MATSUMOTO 6,218,810 in further view of FARRINGTON 6,188,592.

Regarding claim 13.

THEREZE discloses a second control source module, which comprises:

- a first MOSFET transistor (Q1);
- a second MOSFET transistor (Q2);
- a first diode (D1);
- a second diode (D2);



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THEREZE does not disclose

a bias circuit, which provide said first MOSFET transistor and second MOSFET with a fixed bias;

a coupler, which controls states of said diode by an external control signal passing through said coupler.

MATSUMOTO discloses a bias circuit, which provide said first MOSFET transistor and second MOSFET with a fixed bias (figure 10, R1, R2, 52);

FARRINGTON discloses a coupler (Tsx).

It would have been obvious to one having ordinary skill in the art at the time of this invention to provide, a bias circuit, which provide said first MOSFET transistor and second MOSFET with a fixed bias to set the operating conditions of the MOSFETS; a coupler, which controls states of said diode by an external control signal passing through said coupler in order and to isolate the control inputs to the MOSFETS from other parts of the power source module. Regarding claim 14.

The Examiner takes official notice that solid state switching devices such as MOSFETS and IGBT devices are well known in the art. It would have been obvious to one having ordinary skill in the art at the time of this invention to replace the MOSFET transistor with an IGBT to satisfy a design requirement.

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Regarding claims 15, 16.

The Examiner takes official notice:

Coupling devices are well known in the art.

Bias circuits are well known in the art and the components that makeup bias circuits are well known

It would have been obvious to one having ordinary skill in the art at the time of this invention to bias a MOSFET switching device to set the operating conditions of the MOSFET switching device and to couple the control signal through a coupling device such as a transformer or an optical coupling device to isolate the switching control signal from other parts of the circuit.

Any inquiry concerning this communication should be directed to Robert L. DeBeradinis whose number is (703) 306-5857. The examiner can normally be reached on Monday-Friday from 8:30 am to 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus, can be reached on (703) 308-3119. The fax phone number for this Group is (703) 308-7722.

RLD

APRIL 18, 2003

